

WHAT IS CLAIMED IS:

1 1. A method of operating a parallel computer system having
2 at least two processor elements and having a distributed memory,
3 each processor element comprising a local program memory, data
4 memory, communications memory and an operating system, the method
5 comprising the steps of
6
7 (a) in each processor element, globally writing global data and
8 locally reading global data,
9
10 (b) adjoining a global address and/or a number to data written
11 globally,
12
13 (c) for each processor element, determining with an address
14 and/or a number comparator in each processor element on the basis
15 of the address whether the particular processor element is
16 interested in data written globally,
17
18 (d) determining with a local address computation unit a physical
19 address in processor memory when the processor element is
20 interested in the data, and
21
22 (e) establishing parameters of the address and/or number
23 comparator and of the address computation unit in each processor
24 element before or during processing with the operating system.

1 2. A method according to claim 1 including controlling the
2 exchange of messages with a communications manager unit to make
3 possible "zero copying".

1 3. A method according to claim 1 wherein the address
2 comparator comprises one or more address windows, each window

3 comprising an initial address (base) and an end address (top) and
4 that all data within one of these windows are processed further
5 locally.

1 4. A method according to claim 1 including dividing global
2 address space into pages and defining with a table in the address
3 comparator which data are to be processed further locally.

1 5. A method according to claim 4 including adding an
2 offset of one or more bits to a global address to determine a
3 local address.

1 6. A method according to claim 4 including replacing one
2 or more bits of the global address by a base value to determine a
3 local address.

1 7. A method according to claim 4 including forming the
2 table from one or more bits of the global address and/or number
3 and entering a local address value co-determining the address for
4 each table entry.

1 8. A method according to claim 1 including selectively
2 transmitting global writing to selected groups of less than all
3 processors in the system, thereby substantially reducing load on
4 the network.

1 9. A method according to claim 1 wherein barrier
2 synchronization, wherein all processor elements have reached a
3 hit point, is supported by a communications manager unit.

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1 10. A method according to claim 1 including transferring
2 event recognition by a single processor through a communications
3 manager unit to the entire system.

1 11. A method according to claim 1 including supporting one
2 or more exclusive keys with a communications manager unit.

1 12. A method according to claim 1 wherein one or more
2 processor elements act directly as input and/or output elements.

1 13. A parallel computer system comprising
2 at least two processor elements with distributed memory, each
3 processor element comprising a local program memory, a data
4 memory, a communications unit for writing data globally and
5 reading data locally, a communications memory and an operating
6 system, each processor element including a communications manager
7 unit to control the communications unit.

1 14. A parallel computer system according to claim 13
2 wherein each communications manager unit is inserted between each
3 communications unit and a local data transport system of each
4 processor element.

1 15. A parallel computer system according to claim 13
2 wherein each communications manager unit comprises an address
3 comparator and an address computation unit.

ADD A1
ADD B3
ADD O1